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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,485	11/05/2003	Le Trong Nguyen	1397.028000H (SP015.C17)	7752

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
03/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/700,485	NGUYEN ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-11,14-18 and 20-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43-81* is/are allowed.

6)☒ Claim(s) *8-11,14-18 and 20-42* is/are rejected.

7)☒ Claim(s) *20-24 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/14/08, 12/05/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-7,13,19 have been canceled. Claims 8-11, 14-18, 20-42 remain for examination. Claims 43-81 have been added. TD on 01/05/05 has been entered. Upon further consideration, this is action includes new argument of the branch bias. Therefore, it is a non-final action in order to allow applicant chance to respond.

2. Claims 8-12,14-18,25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al. (5,488,729) in view Yoshida (5,481,734).

3. Claims 30-37,41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani et al. (4,942,525) in view of Halo (4,594,655).

4. Claims 38,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani et al. (4,942,525) in view of Halo (4,594,655) in view of Suzuki et al. (5,237,666).

5. The rejections are maintained and incorporated by reference the last Office action on 09/06/07.

6. The response filed on 10/05/07 has been fully considered but is not persuasive.

7. In the remarks , applicant argued that :

a) "a register rename circuit configured to provide references to locations in the register file for logical register references included with the plurality of buffered instructions," as recited in claim 8.

b) Vegesna does not teach branch bias that enable microprocessor to process a conditional branch instruction by either assuming the branch will be taken or assuming the branch will not be taken; Vegesna's architecture simply assumes a branch will not be taken

c) examiner has failed to even acknowledge any above-described differences between claim 8 and Vegesna and Yoshida;

d) Shintani nor Hao teach or suggest "retiring the instruction group held in the multiple-stage buffer" and "advancing an other instruction group held in the multiple-stage buffer" as currently recited in independent claim 30.

8. As to a) above, Vegesna taught a register rename circuit configured to provide references to locations in the register file for logical register references included with the plurality of buffered instructions," as recited in claim 8 (see the renamed destination and source registers and the unit which generated them as the rename circuit in col.13, lines 57-67). The destinations and sources were the references to locatons in the register file for logical register references (e.g. the renamed registers). Vegesna taught clearly destination and source registers being renamed. If register renamed not being done by rename circuit , what else could it be ?

9. As to b), applicant never claims enabling microprocessor to process a conditional branch instruction by either assuming the branch will be taken or assuming the branch will not be taken. Applicant only recites : a branch bias signal indicating whether a conditional branch controlled by a conditional branch instruction is predicted to be taken or not taken. One of ordinary skill in the art should be able to recognize Vegesna's architecture was applicable to a branch bias for predicting taken or not taken.

10. As to c) above, see response to b) above.

11. As to d), Shintani taught the completion of the execution cycle in co1.5, lines 65-68, co1.6, lines 1-7). Therefore, it was directed to the retirement of the instruction.

12. As to the "advancing an other instruction group held in the multiple-stage buffer" as currently recited in independent claim 30, Shintani taught a completion of the instruction execution cycle (see col.5, lines 65-68, col.6, lines 1-7). Therefore, the corresponding contents of the registers must be advanced in a forward direction by

number of stages (or prefetch, read, decode cycles etc.), otherwise, the completion cycle would not have been reached.

13. Claims 20-24 are objected to as being dependent upon a rejected base claim, for reciting the details of the retirement of the control, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claim 39 is objected to as being dependent upon a rejected base claim, for reciting further details of the register file and the execution of outside order and the temporary buffer, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Claims 43-62 are allowable over the art of record for reciting combined features of :

a) an instruction fetch unit configured to fetch instructions from an instruction store (IB1 IB2) according to a sequential program order; and

b) an instruction execution unit configured to concurrently receive a set of from 1 to a maximum number of instructions from the instruction fetch unit, the instruction execution unit including:

an instruction buffer configured to store instruction information for each instruction received from the instruction fetch unit, wherein the instruction buffer has sufficient capacity to store the instruction information for at least twice the number N of instructions;

c) a register file comprising a plurality of temporary buffers and a plurality of retired registers, the temporary buffers are arranged in a plurality of groups of temporary buffers, each group of temporary buffers including N of the temporary buffers;

renaming logic configured to concurrently establish an association

between each instruction in a set of instructions concurrently received from the instruction fetch unit and a respective one of the temporary buffers in a selected one of the groups of temporary buffers, wherein a position of each instruction within the set of instructions determines which one of the temporary buffers in the selected group of temporary buffers is associated with that instruction;
d) a plurality of functional units configured to execute instructions, thereby generating result data;
an issue control circuit configured to concurrently issue more than one of the instructions for which instruction information is stored in the instruction buffer to the functional units for execution, the issue control circuit being further configured to issue at least some of the instructions out of the sequential program order;
e) a plurality of data routing paths coupled between the functional units and the register file and configured to transfer result data from more than one of the functional units to the temporary buffers concurrently; and
f) retirement control logic coupled to the register file and configured to retire instructions according to the sequential program order, wherein the retirement control logic is further configured to concurrently retire all of the instructions in a set of instructions after all of the instructions in that set of instructions have completed.

claims 63-81 are allowable for the combined features of :
a) fetching instructions from an instruction store according to a sequential program order;
b) concurrently delivering a set of from 1 to a maximum number (N) of fetched instructions to an instruction execution unit, wherein the instruction execution unit includes a register file comprising a plurality of temporary buffers and a plurality of retired registers, wherein the temporary buffers are arranged in a plurality of groups of temporary buffers, each group of temporary buffers including N of the temporary buffers;
c) storing instruction information for each instruction in the set of delivered instructions

in an instruction buffer of the instruction execution unit, wherein the instruction buffer has sufficient capacity to store the instruction information for at least twice the number N of instructions;
d) concurrently establishing an association between each instruction in the set of instructions delivered by the instruction fetch unit and a respective one of the temporary buffers in a selected one of the groups of temporary buffers, wherein a position of each instruction within the set of instructions determines which one of the temporary buffers in the selected group of temporary buffers is associated with that instruction;
concurrently issuing more than one of the instructions for which instruction information is stored in the instruction buffer to a plurality of functional units, wherein at least some of the instructions are issued out of the sequential program order;
executing the issued instructions in the plurality of functional units, thereby generating result data;
e) concurrently transferring the result data from more than one of the plurality of functional units to the temporary buffers; and
f) concurrently retiring all of the instructions in the set of instructions after all of the instructions in the set of instructions have completed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

/Daniel Pan/
Primary Examiner, Art Unit 2183